MULTI-CHANNEL MAGNET POWER-SUPPLY RAMP CONTROLLER FOR THE IUCEEM ALPHA SYNCHROTRON/STORAGE RING WITH CHANNEL ACCESS

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Abstract

A four-channel magnet-power-supply ramp controller has been designed and deployed at the new ALPHA (Advanced Electron Photon Facility) at the Indiana University Center for Exploration of Energy and Matter (IUCEEM). The first application is a power-supply controller. For all practical purposes, the system is a versatile arbitrary voltage-waveform-generator with full DAQ (data acquisition) capabilities that can be used in a variety of beam instrumentation settings. The real-time controller can generate four arbitrary independently-triggerable ramp profiles. A normalized wave-form vector is encoded as a Process Variable array and is uploaded and stored by the real-time controller as required. Each ramp array element is clocked out to a 16-bit DAC (Digital to Analog Converter) via a DMA FIFO and built-in FPGA. The duration of the waveform is programmable with a minimum time resolution of 20 µsec between profile values. Four bipolar DACs have an output range of +/- 10V. Eight digital I/O control bits are allocated for each control channel. Typically, these bits are used to monitor and control the power-supply operational state. The control-system interface uses the EPICS Channel-Access server accessible on Labview RT 2009.

ALPHA STORAGE RING

The Advanced eLectron PHoton fAcility (ALPHA) consists of an electron LINAC coupled to a storage ring which will provide the beam to a device test area[1]. Ultimately, it will provide a 20 MeV 68 mA electron beam. ALPHA is under construction at this time, commissioning is planned for the second quarter of 2010. There are a number of operating modes. In one mode of operation, the storage ring would modify the pulse structure to eliminate bunching of electrons emerging from the LINAC[2]. In another mode, the storage ring will capture bunches of electrons and compress their time width to provide high-intensity electron pulses. ALPHA will be capable of providing X-rays using high-efficiency Bremsstrahlung targets or by Inverse Compton Scattering.

This multi-mode operation requires beam management via sophisticated programmable power-supply control electronics.

The controller described below is an example of a system whose software and hardware architecture can be used as a versatile arbitrary voltage-waveform-generator with full DAQ (data acquisition) capabilities that can be deployed for a variety of beam instrumentation applications.

POWER SUPPLY RAMPING AND CONTROL REQUIREMENTS

The ALPHA storage ring requires a number of magnets to ramp their magnetic fields in response to a timing pulse. Four main dipoles are wired in series and are excited by a single 20 kW power supply. Other magnets, such as correctors and quadrupoles have individual supplies controlled and monitored by the system that will be described.

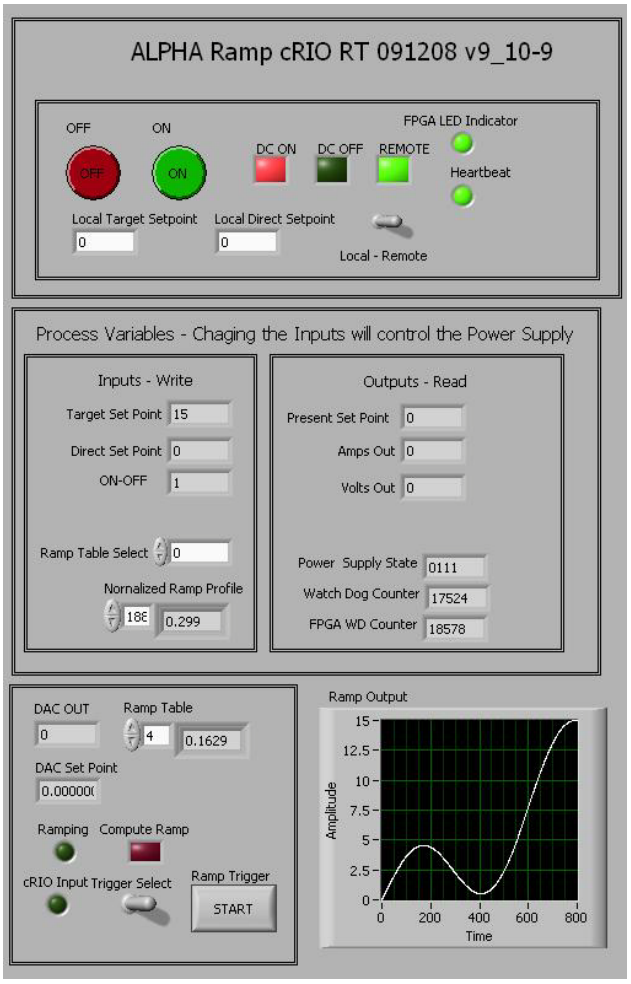

Figure 1. ALPHA ramping control panel

Each magnet is required to ramp from an initial to final magnetic field value following a specific ramp profile in one second. This ramp period may be longer during certain operations. Ramp initiation latency, the time between the trigger and ramp start must be less than 300 µsec. All of the power supplies in the system run in the constant-current mode and require an analog programming voltage of 0-10 V. In addition to the ramping waveform, the power-supply controller must monitor output voltage and current, and act as the state-machine [3] for each power-supply channel. This allows remote control and monitoring of power supply states, and interlock faults.

All controllers communicate with the accelerator control system using EPICS Channel-Access protocol [4].

CONTROL AND DATA-ACQUISITION TOPOLOGY

National Instruments cRIO and FPGA

The controller uses National Instruments (NI) hardware chassis (See Figure 1) based upon NI's Compact RIO (reconfigurable I/O), cRIO, and architecture. Physical connections are achieved through a series of BiRIO interface wiring cards[5] housed in a 19"-4U chassis.

The system architecture consists of four major parts. Real-time controller

1. Chassis-mounted signal conditioning modules
2. A Virtex II FPGA (field programmable gate array) that is the intermediate processor between the RT and the I/O modules.
3. Ethernet interface.
4. Channel-Access Server

The power of this configuration is contained in the FPGA which can run multiple, simultaneous processes. This is a true parallel process environment at a minimum of 40 MHz. See Figure 2.

The advantage of this arrangement is that the FPGA is programmed in Labview, not VHDL. Two pieces of software must be written, but all use the common graphical programming paradigm of Labview, the virtual instrument (VI). Labview FPGA contains all of the components to load and run the FPGA code.

The DAC ramping, hence power-supply ramping, is triggered and executed in the FPGA. he ramp profile data vector is calculated by the Real-Time processor and is sent to the FPGA via DMA transfer. The data rate is limited only by the PCI parallel bus speed, which is 33 MHz.

Ramp Vector Generation

The required capability of the controller is to deliver an arbitrary ramp waveform to the power supply. The power supply – magnet pair will create a time-dependent magnetic field. The beginning and end point values of the field are also arbitrary and can change with each time the ramp is executed. The shape of the ramp needs to remain the same. We have chosen to model the ramp as a normalized ramp vector, whose values can vary from 0 to 1. A utility program was written to convert a waveform to the normalized form. This allows the modelling without being constrained by the limits of the hardware. See Figure 3.

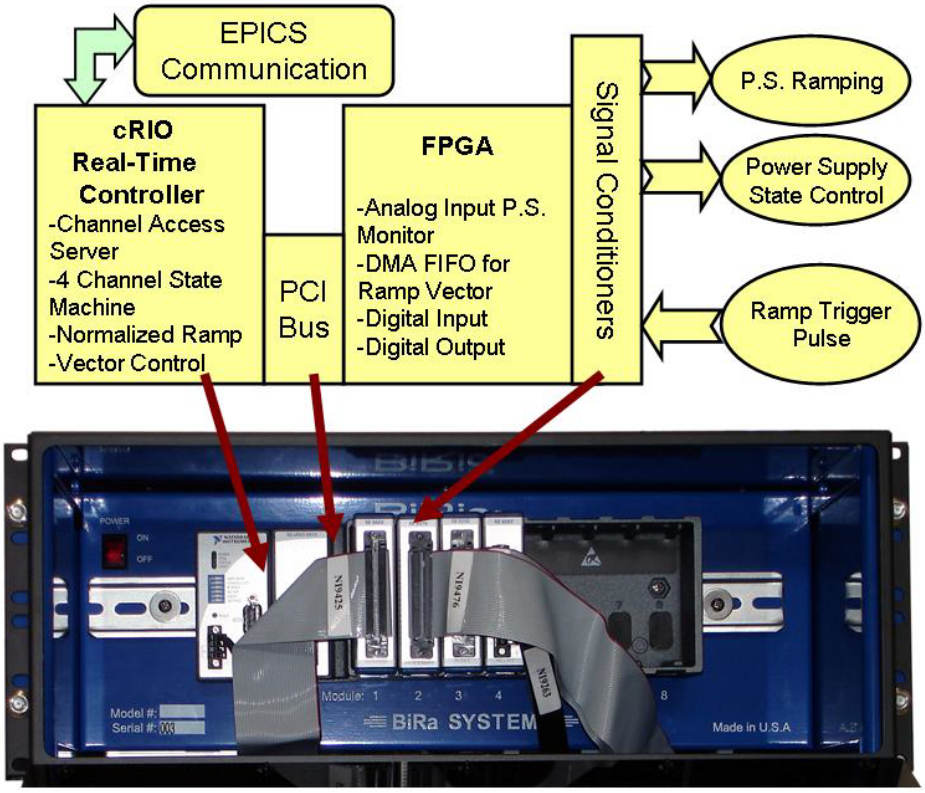

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Figure 2 Real Time Architecture and cRIO hardware

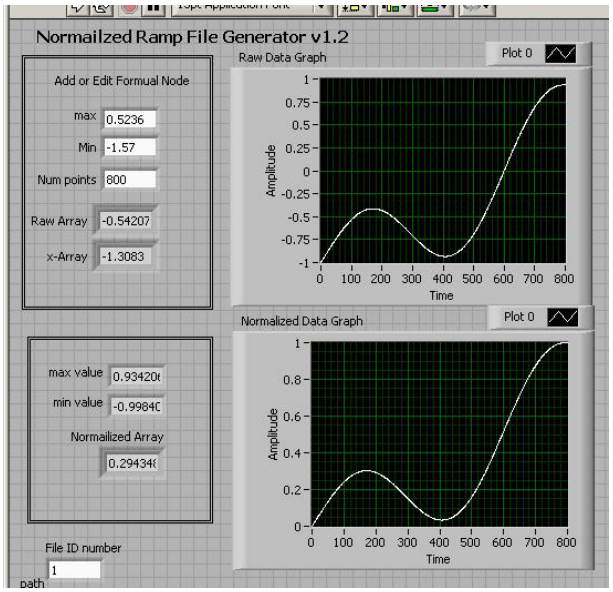

Figure 3 Normalized ramp vector generator. Compare the ordinate (y-axis) between the upper and lower graph. This shows the function: y =sin(x) +0.5sin(4x);

CHANNEL ACCESS INTERFACE

The most current version of Labview contains an Channel-Access server module that allows one to bind Labview shared variables to EPICS process variables (PV). This means that, shared variables are immediately accessible to the EPICS control system. A large number of process variable data types are allowed including floating point arrays. Arbitrary ramp vectors do not need to be stored on the cRIO real time processor, since they can be uploaded in a millisecond when required. The original design of the system was to store multiple ramp vectors on each controller for each power supply channel. The capability of the on-demand ramp profile change reduces configuration management tasks, since all of the profiles are stored at one central location.

Figure 4 shows the mapping of Labview shared variables to Channel-Access variables. Once the Real Tim application and the EPICS server are running on the cRIO processor, the PV's are immediately accessible via "caget" and "caput" [6] commands.

For development we wrote a control program that runs on a MS Windows XP computer using both LV shared variables and channel access variables. Both approaches worked provided reliable communications and control.

PV	Access Type	Variable Path	Data Type
10.1.1.227:EPICS_Ramp_PV_2:NRampData	Read/Write	IUCMB-ALPHA-3\EPICS Ramp PV 2.lvlib	Array of Double
10.1.1.227:EPICS_Ramp_PV_2:alvled	Read/Write	IUCMB-ALPHA-3\EPICS Ramp PV 2.lvlib	Boolean
10.1.1.227:EPICS_Ramp_PV_2:FPGALED	Read/Write	IUCMB-ALPHA-3\EPICS Ramp PV 2.lvlib	Boolean
10.1.1.227:EPICS_Ramp_PV_2:RampDataSz	Read/Write	IUCMB-ALPHA-3\EPICS Ramp PV 2.lvlib	Int32
10.1.1.227:EPICS_Ramp_PV_2:WDCntr	Read/Write	IUCMB-ALPHA-3\EPICS Ramp PV 2.lvlib	UInt32
10.1.1.227:EPICS_Ramp_PV_2:RemDirectStpt	Read/Write	IUCMB-ALPHA-3\EPICS Ramp PV 2.lvlib	Double
10.1.1.227:EPICS_Ramp_PV_2:RemTartetStpt	Read/Write	IUCMB-ALPHA-3\EPICS Ramp PV 2.lvlib	Double
10.1.1.227:EPICS_Ramp_PV_2:remonoff	Read/Write	IUCMB-ALPHA-3\EPICS Ramp PV 2.lvlib	UInt16
10.1.1.227:EPICS_Ramp_PV_2:RemRampTrig	Read/Write	IUCMB-ALPHA-3\EPICS Ramp PV 2.lvlib	Boolean

Figure 4. EPICS process-variable mapping.

CRIO CONTROLLER COMPONENTS

cRIO platform

We chose a integrated cRIO controller with four I/O modules for this application. National Instruments make a number of controllers with increasing levels of computing power and FPGA with increasing numbers of gates. The more powerful units have a separate controller with a PCI bus, to which one can attach a back plane that contains the FPGA. This allows one to match the controller and gate array to a specific application. We chose the NI model 9073 which has the real-time controller and FPGA on a single printed circuit board. The unit has a modest 266 MHz Freescale processor, Ethernet 10BaseT port, and a single RS-232 port. Labview Real-Time is built on top of Wind River Systems, VxWorks operating system. The serial port can be allocated as a console port to monitor the controller and have some limited access to the VxWorks operating system. Be aware that not all functions of VxWorks are accessible. The system includes four I/O modules, one each of 32-channel digital input unit, 32-channel digital output unit, 32-channel multiplexed 16-bit analog to digital converter (ADC) and four-channel 16-bit digital to analog converter (DAC).

The modules should be thought of as signal conditioners. The main job of the modules is to create a digital signal that can manipulated by the FPGA. This gives the user tremendous flexibility, while trading off the

option of having the I/O modules working “right out of the box.”

REAL-TIME OUTPUTS

. The real-time controller can generate four arbitrary independently-triggerable ramp profiles. Each profile element is clocked out to a 16-bit DAC via a DMA FIFO and built-in FPGA. The duration of the waveform is programmable with a minimum time resolution of 20 µsec between profile values. Four bipolar DACs have an output range of +/- 10V. Eight digital I/O control bits are allocated for each control channel. Typically, these bits are used to monitor and control the power-supply operational state.

For practical purposes, the system is a versatile arbitrary voltage-waveform-generator with full DAQ (data acquisition) capabilities that can be used in a variety of beam instrumentation settings. The real-time controller can generate four arbitrary independently-triggerable ramp profiles. See Figure 5.

Figure 5 Actual DAC (analog-voltage output) ramp profiles.

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