

LA-UR-11-10180

Approved for public release; distribution is unlimited.

Title: Upgrading the Data Acquisition and Control System of the LANSCE LINAC

Author(s): Baros, Dolores

Intended for: Particle Accelerator Conference 2011, 2011-03-28/2011-04-02 (New York, New York, United States)



Disclaimer:

Los Alamos National Laboratory, an affirmative action/equal opportunity employer, is operated by the Los Alamos National Security, LLC for the National Nuclear Security Administration of the U.S. Department of Energy under contract DE-AC52-06NA25396. By acceptance of this article, the publisher recognizes that the U.S. Government retains nonexclusive, royalty-free license to publish or reproduce the published form of this contribution, or to allow others to do so, for U.S. Government purposes. Los Alamos National Laboratory requests that the publisher identify this article as work performed under the auspices of the U.S. Department of Energy. Los Alamos National Laboratory strongly supports academic freedom and a researcher's right to publish; as an institution, however, the Laboratory does not endorse the viewpoint of a publication or guarantee its technical correctness.

UPGRADING THE DATA ACQUISITION AND CONTROL SYSTEM OF THE LANSCE LINAC

D. Baros, LANL, Los Alamos, NM 87545, U.S.A.

Abstract

Los Alamos National Laboratory LANL is in the process of upgrading the control system for the Los Alamos Neutron Science Center (LANSCE) linear accelerator. The 38 year-old data acquisition and control equipment is being replaced with COTS hardware. An overview of the current system requirements and how the National Instruments cRIO system meets these requirements will be given, as well as an update on the installation and operation of a prototype system in the LANSCE LINAC.

LANSCE

LANSCE is a National Research Facility which contains a half-mile-long linear accelerator (LINAC). The LANSCE LINAC creates proton beams with energies up to 800 million electron volts and is capable of accelerating protons to 84% the speed of light. LANSCE achieved full energy on June 9, 1972 and continues to run to this day with much of its late 1960's – early 1970's technology intact. An example of this late 1960's technology is the data acquisition and control system for the LANSCE LINAC better known as RICE (Remote Indication and Control Equipment).

RICE

RICE was built as part of the first large-scale efforts to use computers to control an accelerator. Designed in the late 1960s, before CAMAC and VME standards, it was created to provide control and data readout for most devices in the LANSCE LINAC. Its architecture was designed to directly map onto the architecture of the LINAC and thus is tightly coupled to the LINAC hardware. An average RICE module contains 30 analog inputs, 50 binary inputs, 8 analog commands, and 30 digital command channels. There are 66 RICE modules distributed along the LANSCE LINAC. The layout of the LANSCE LINAC is illustrated in Figure 1. The 66 RICE Modules are connected to one uVAX computer in a star topology configuration.

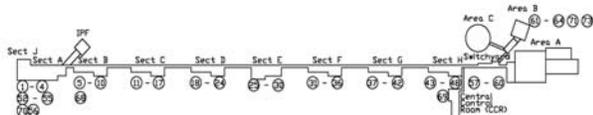


Figure 1: LANSCE LINAC.

A RICE module consists of three separate components: the RICE chassis, the RICE Input/Output (I/O) chassis and the Analog Data System (ADS) chassis. The RICE chassis is a serial to parallel and parallel to serial word encoder/decoder. The RICE I/O chassis is used to

interface the RICE system with the accelerator inputs/outputs. It can address up to 128 binary channels. The ADS chassis is a 128 channel differential A/C converter used for analog readback of accelerator devices.

Interface between the RICE system and accelerator equipment is accomplished through a distribution panel located on the side of the equipment rack. Owners of the equipment run wires to this distribution panel to connect with the RICE hardware.

RICE Controls

RICE controls can be split into two main categories, Industrial Controls and Timed-and-Flavored Data. Industrial Controls consist of command and readback of two-state devices, along with set-point generation and analog readback of devices. Timed-and-Flavored data provides data with a time correlation related to the operation of the accelerator. This paper discusses the replacement of the RICE Industrial Controls (IC).

Problems with RICE upkeep

There are several problems that arise due to the RICE system being designed with 30 year old technology. The supply of spare RICE IC replacement boards is dwindling or has been spent. Many of the discrete components that make up the RICE electronics can no longer be purchased. The plastic connectors on the RICE printed circuit boards are becoming brittle and spares are not available. Calibration capabilities were not built-in to the system, raising questions about year-to-year comparability of settings. Lack of any vendor support means all maintenance and repairs must be done in-house. The use of non-standard electronics means all in-house people must receive extensive RICE-specific training. The original designers and builders have retired making extended re-engineering necessary to understand the reasons for current architecture. Although RICE is very reliable, it is long past its expected lifetime and the lack of spares makes the probability of eventual catastrophic failure real.

UPGRADE REQUIREMENTS

The RICE system is required for the operation of the LANSCE LINAC functional requirements and constraints for the RICE upgrade are as follows:

- Avoid serious failures due to age of system and lack of spares.
 - A serious failure due to RICE would impact beam availability for users.
- Growth path for a 30 year facility life expectancy.

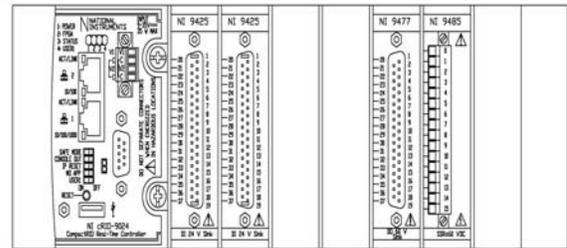
- Plans for the LANSCE accelerator to be used as the proton beam source for the Matter-Radiation Interactions in Extremes (MaRIE) experimental facility project a 30 year lifetime for the facility.
- High Reliability
 - The new system should have an expected downtime no worse than the existing RICE
- Support and use outside the accelerator community so we can benefit from development by others.
 - A commercial modular system is desirable for low mean-time-to-repair and vendor support.
- No extended accelerator downtimes force by upgrade project.
 - The upgrade must not require downtimes beyond normally scheduled monthly maintenance and extended maintenance periods.
- RICE functionality must be preserved or improved.
 - Analog input data with 11 bits plus sign.
 - Analog input ranges from $\pm 10V$, $\pm 1 V$, $\pm 100 mV$
 - Analog commands must be compatible with existing stepper motor controllers.
 - Binary input data, compatible with 0-8.5V for low and greater than 14V for high.
 - Binary commands compatible with existing local binary command modules.
 - Linked binary commands: command to one channel may command others.

RICE REPLACEMENT

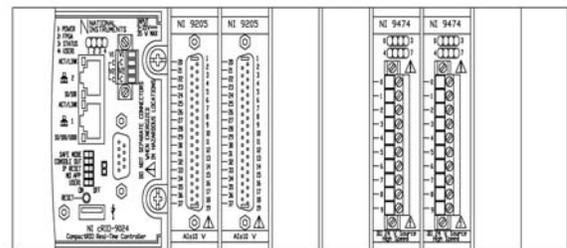
Programmable Automated Controllers (PACS) specifically National Instruments (NI) Compact RIO (cRIO) PACS system was chosen to replace the RICE IC. The cRIO system was able to meet or exceed the system requirements necessary for the RICE IC replacement. The cRIO system is a reconfigurable control and data acquisition system. It is a high performing system that is very reliable with individual module “Mean Time Before Failure” MTBF ranging from 37,141 hours. to 2,172,740 hours [1]. It is a commercial modular system that is being used in a wide range of applications from Avionics to robotics. Because each cRIO system is independent of other cRIO system connected in a bus topology, we will be able to replace the RICE system in sections during scheduled maintenance periods. The cRIO system has a variety of hot swappable I/O modules that can be used for a variety of applications which correspond to the RICE functionality requirements.

The cRIO system functionality will be divided up between one analog chassis and one digital chassis. The analog chassis will consist of the set-point generation controls and the analog readback of devices. The digital chassis will consist of the command and readback of two-state devices. Each chassis will contain a cRIO-9024

real-time powerPC controller, a cRIO-9118 8-slot kVirtex-5 LX110 reconfigurable chassis, applicable I/O modules, corresponding I/O terminal interface boards and a prewired rack mountable chassis enclosure. The layout of the cRIO Analog and Digital Chassis is illustrated in Figure 2.



RICE REPLACEMENT DIGITAL CHASSIS



RICE REPLACEMENT ANALOG CHASSIS

Figure 2: cRIO Digital and Analog chassis.

IMPLEMENTATION OF CRIO

Binary Channel Implementation

RICE Module 48 was chosen to test cRIO prototype system. Two “Variable Energy” binary output channels were selected to be installed because of their critical switching time constraint. It was a do-or-die test for the cRIO system. These channels were installed and successfully tested in November of 2008. The remainder of the binary command and readback channels were implemented in May of 2009. The cRIO system consisted of the following components:

- NI cRIO-9014 – Real time controller with 400 MHZ, 128 MB DRAM and 2 GB storage.
- NI cRIO-9103 – 4-slot chassis with an embedded 3 M gate Virtex-II FPGA
- NI-9425 – 32-channel, 24V sinking digital input module
- NI-9477 – 32-channel, 5V to 60 V sinking digital output module
- In-house built rack mount bracket
- Generic interface boards
- LabVIEW 8.5

Problems with Binary Channel Implementation

One of the problems that we encountered with the implementation of the binary channels was that the embedded Experimental Physics and Industrial Control

System (EPICS) software that is used at LANSCE, was only tested on LabVIEW 8.5. LabVIEW 2009 was available to program the cRIO code, but because the EPICS software had not been tested on LabVIEW 2009, we were forced to use the older software. Use of this older software caused a second problem, we ran out of FPGA memory. The LabVIEW program for the binary channels used up 99% of the FPGA space. Time was our third problem. We were limited on the amount of time that we had to install and test the binary cRIO by the accelerator maintains period. The last problem we encountered was that we connected the NI-9477 binary output module to a piece of accelerator equipment that was not tied to ground. This caused the NI-9477 module to fail.

Binary Implementation Corrections

We were able to address these problems that arose in our implementation of the binary channels. NI finished its testing of the LabVIEW 2009 software with embedded EPICS and released it to us. The FPGA space problem was solved by replacing the cRIO controller and chassis with the NI cRIO-9024 controller (800Mhz, 512 MB DRAM and 4GB storage). The NI-9485, 8-channel solid-state relay digital output module, was installed to interface with the accelerator channels that were not tied to ground. This eliminated the problem with the NI-9477. To improve on the time needed to install a cRIO system, we purchased a commercial BiRIO rack mount chassis and BiRIO terminal interface boards.

Implementation of Analog Channels

The analog chassis for Module 48 was installed in May of 2010. The cRIO system consisted of the following components:

- NI cRIO-9024 – Real time controller with 800MHZ, 512 MB DRAM and 4 GB storage.
- NI cRIO-9118 – 8-slot chassis with Virtex-5 LX110 FPGA
- NI-9205 – 32-channel, 16-Bit analog input module configured as a 16 channel differential analog input module.
- NI-9474 – 8-channel, 5 -30V digital output module used to create 5V, 50us wide pulses for stepper motors
- BiRio-FS9010 – BiRa 19” rack mount cRIO chassis
- BiRio- Interface boards
- LabVIEW 2009

Problem and Corrections with Analog Channels

Only one problem arose with implementation of the analog channels, noise on the input signals.

Our first approach to solving the analog input noise problem was to connect all unused input channels to ground on the interface board. This improved the noise problem slightly. We then installed an RC filter at the interface junction going to the input channels to the cRIO module. This eliminated more of the noise but another

solution was needed. Finally we installed a 2 pole Butterworth Filter to the software input of the module. The combination of these three solutions eliminated the noise problem. The flow diagram of the cRIO system is illustrated in Figure 3.

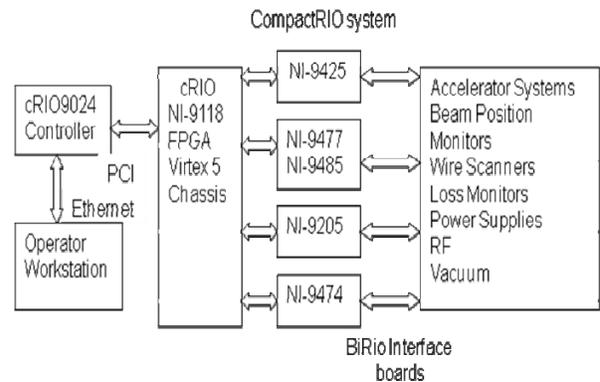


Figure 3: cRIO system.

CONTINUED RICE UPGRADE

Current Upgrade

Due to the modular nature of the cRIO system, it will be installed in smodules during the LANSCE LINAC maintenance periods. For the current maintenance period, Sector H of the LANSCE LINAC was chosen to be upgraded. Sector H, illustrated in Figure 1, consists of RICE Modules 43- 47. RICE Module 47 is currently being worked on with the subsequent Sector H RICE modules to follow.

Improvements

We have worked with BiRa Systems [2] to amend the interface board for the NI-9205 module (analog input) so that now the RC filter can be installed on the board rather than the interface junction to the module. BiRa has also enhanced their BiRio-FS9010 rack mount chassis to a functional pre-wired cRIO system chassis. This will help decrease our time needed for during the installation of cRIO systems.

FUTURE RICE UPGRADE

RICE Modules will be upgraded in sections, preferably a sector at a time. As funding becomes available, we will continue to upgrade the RICE IC system to the cRIO system.

REFERENCES

- [1] National Instruments CompactRIO
- [1] BiRa Systems, Albuquerque, NM

